

FIG. 1

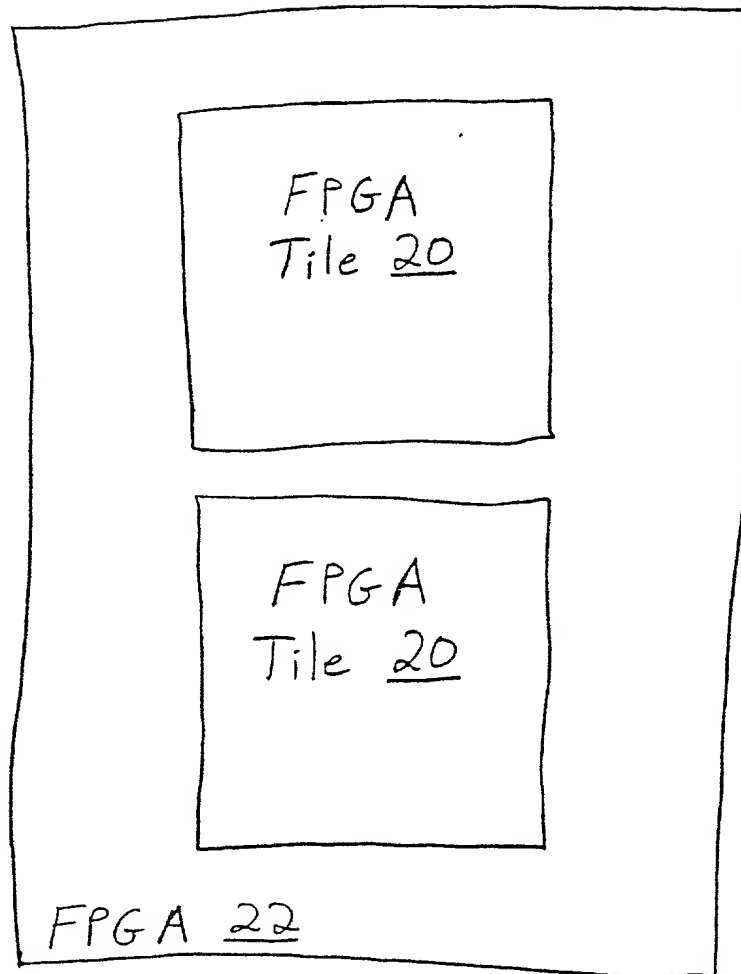


FIG. 2

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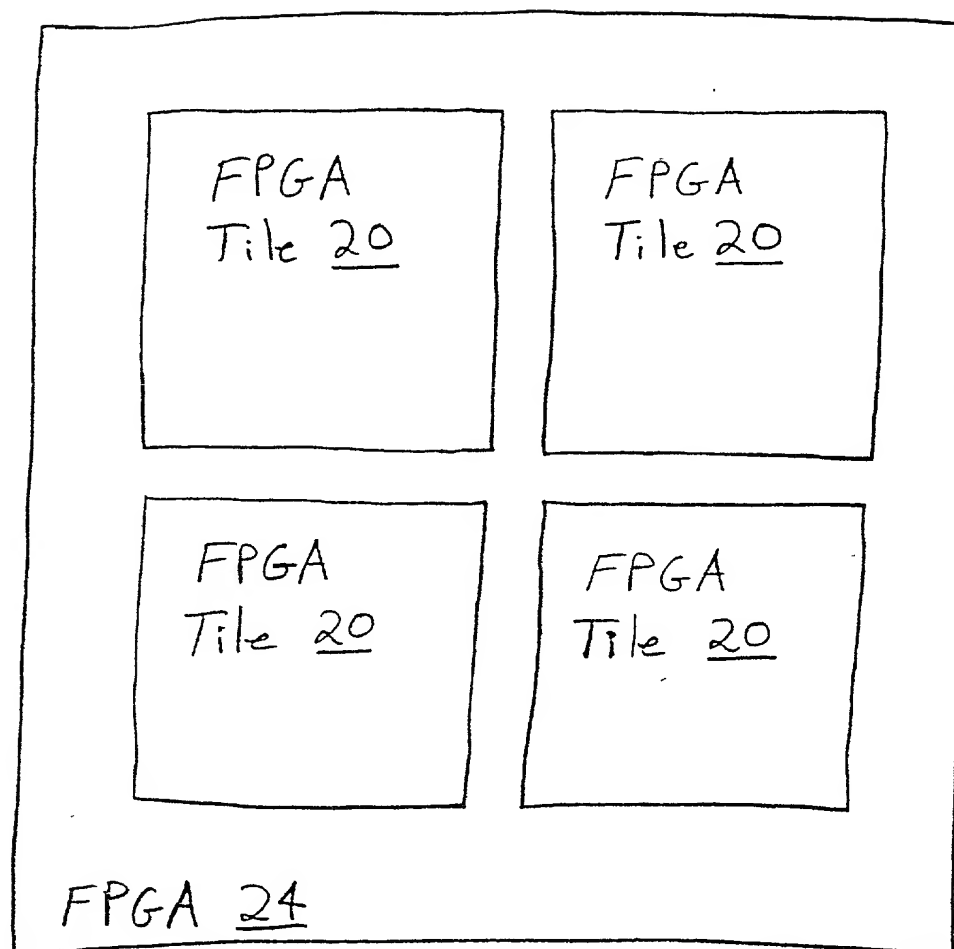


FIG. 3A

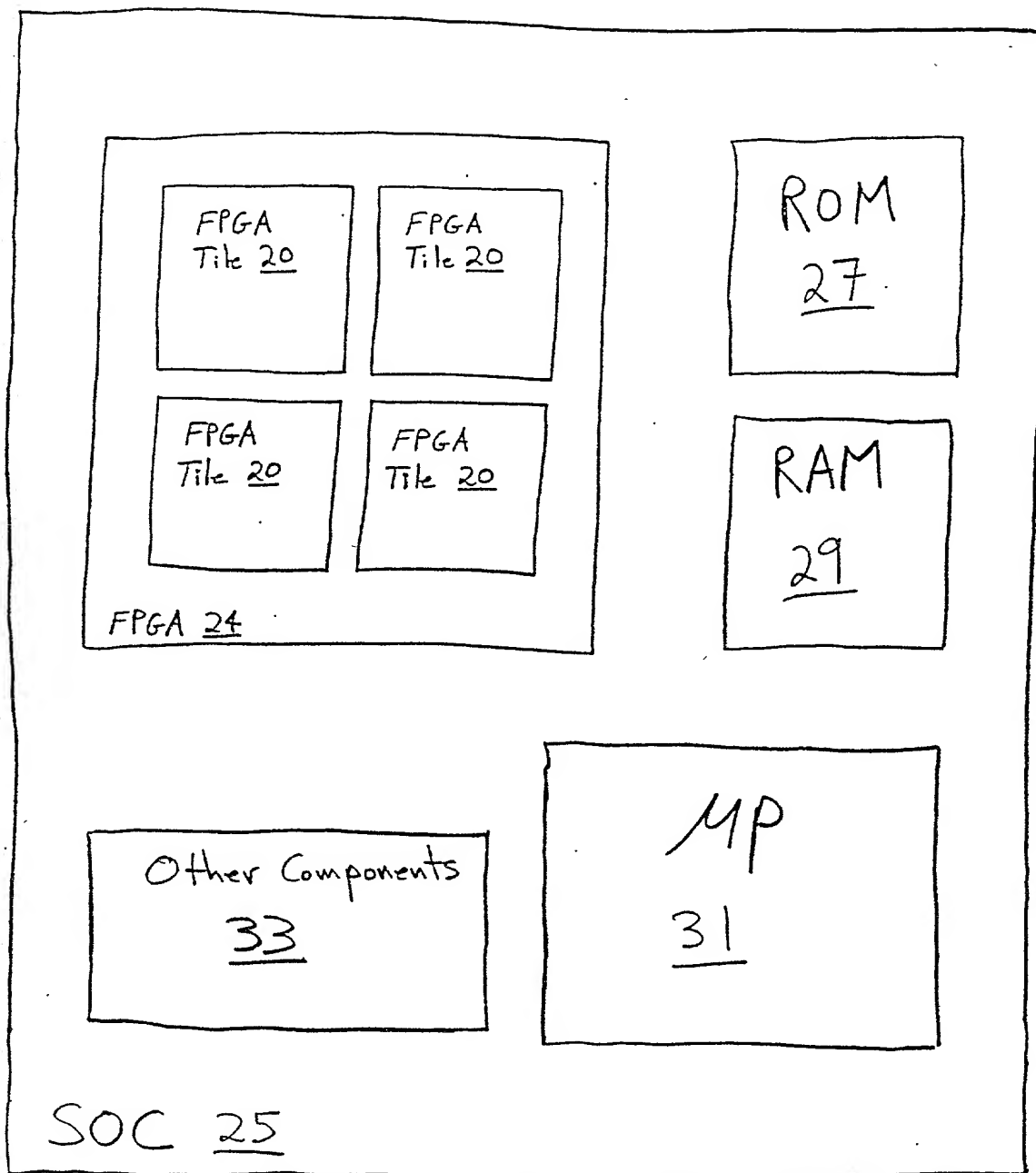


FIG. 3B

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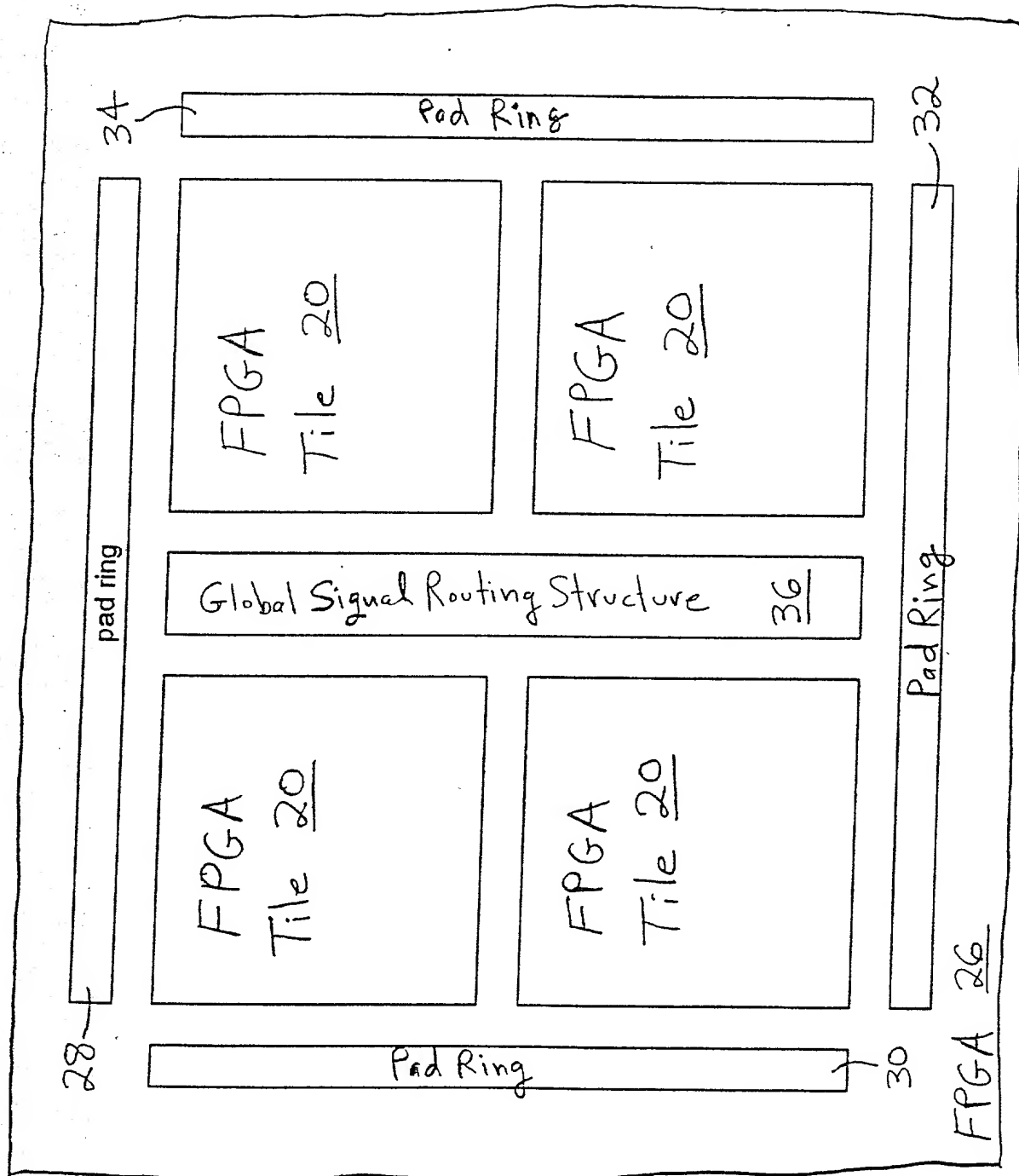


FIG. 4

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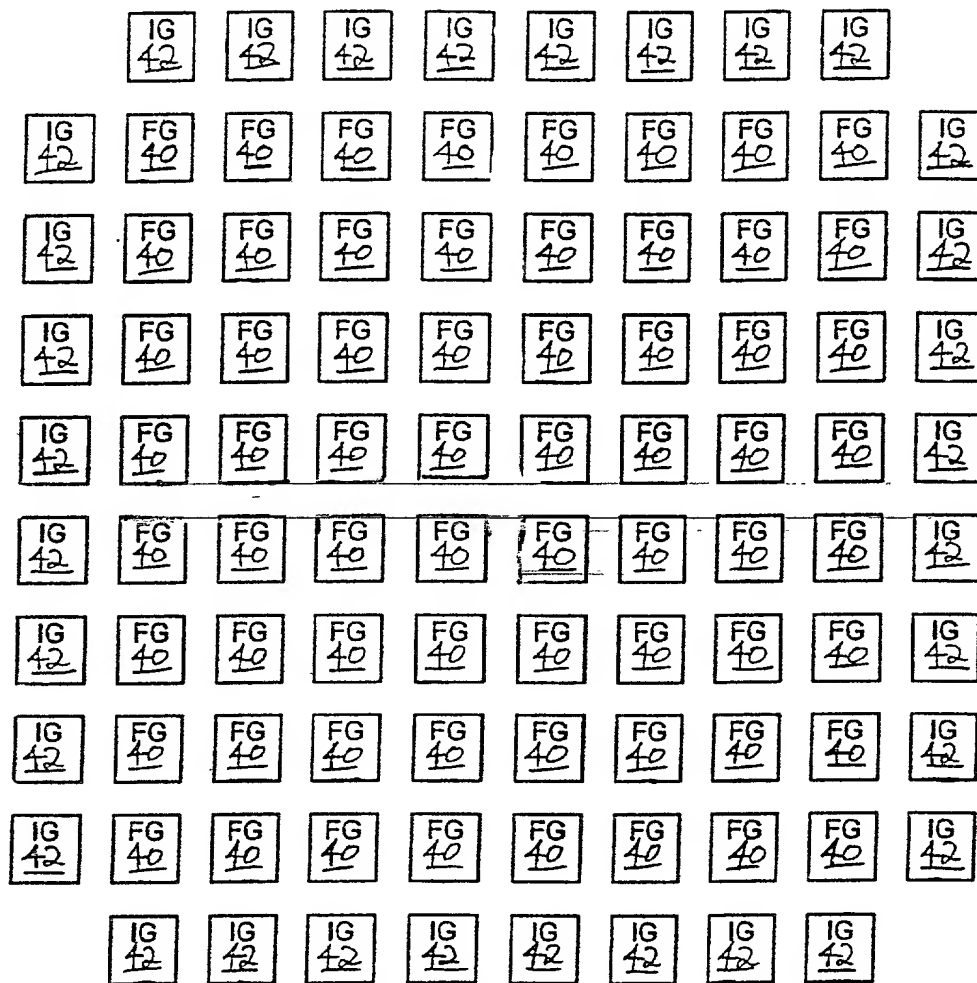


FIG. 5

1007400730

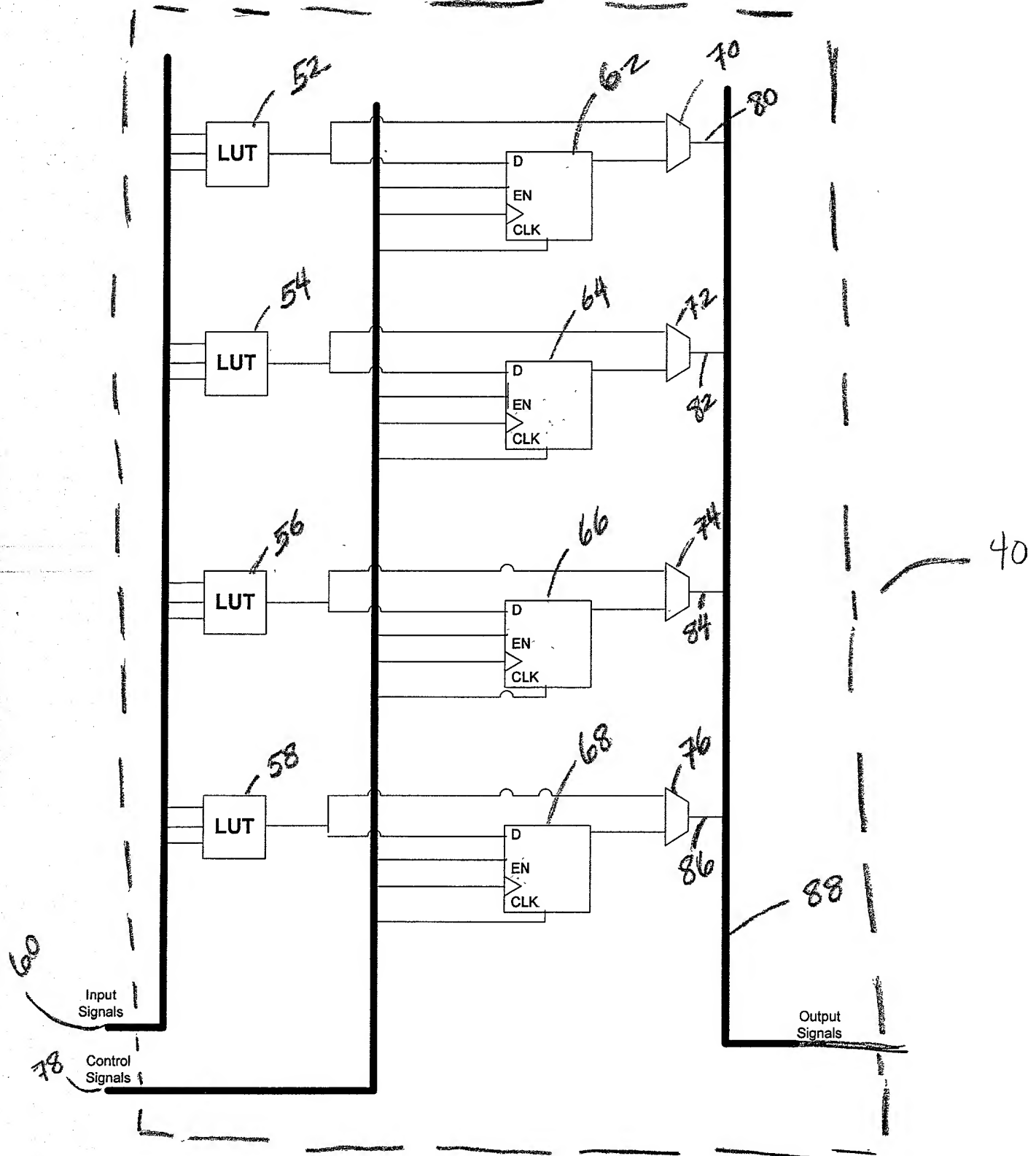


FIG. 6

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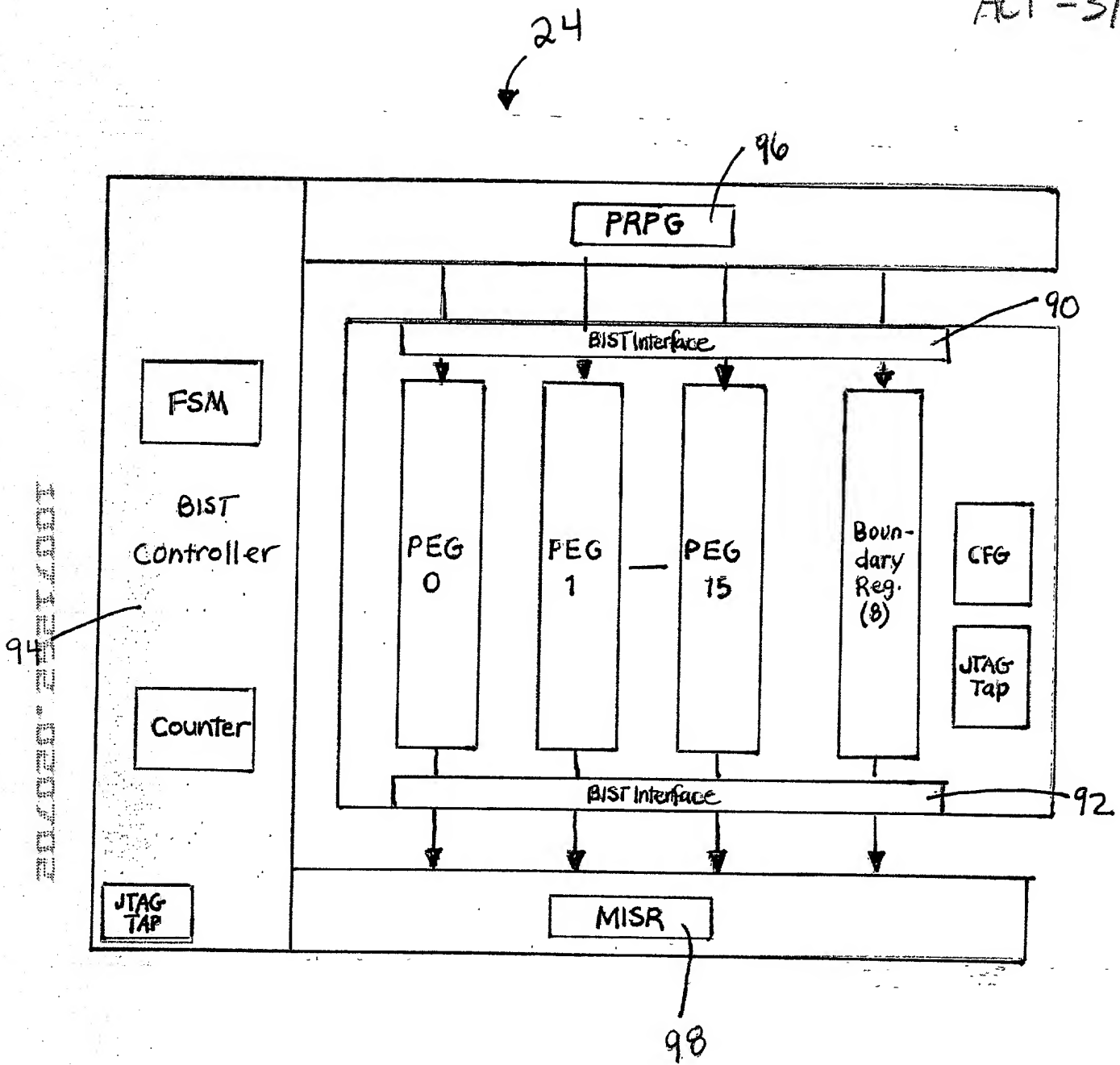


FIG. 7



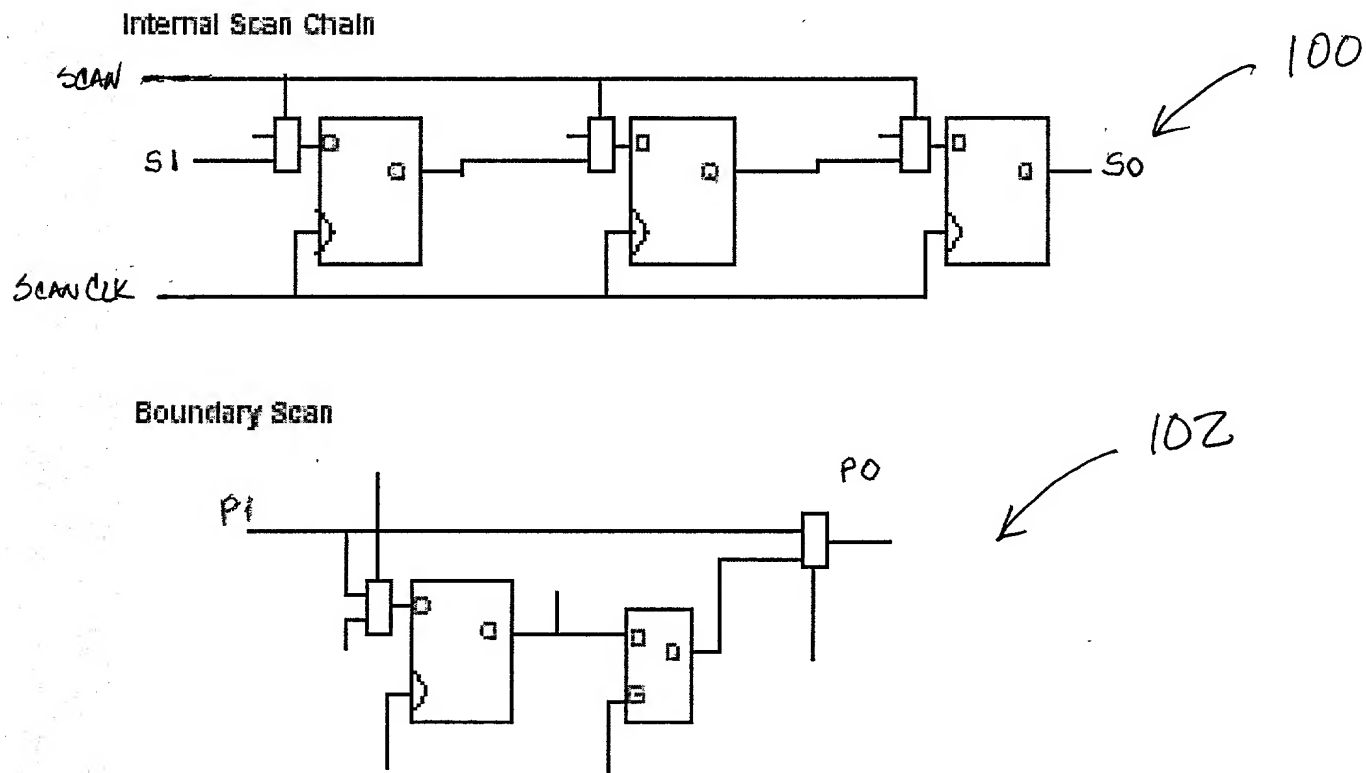


FIG. 8

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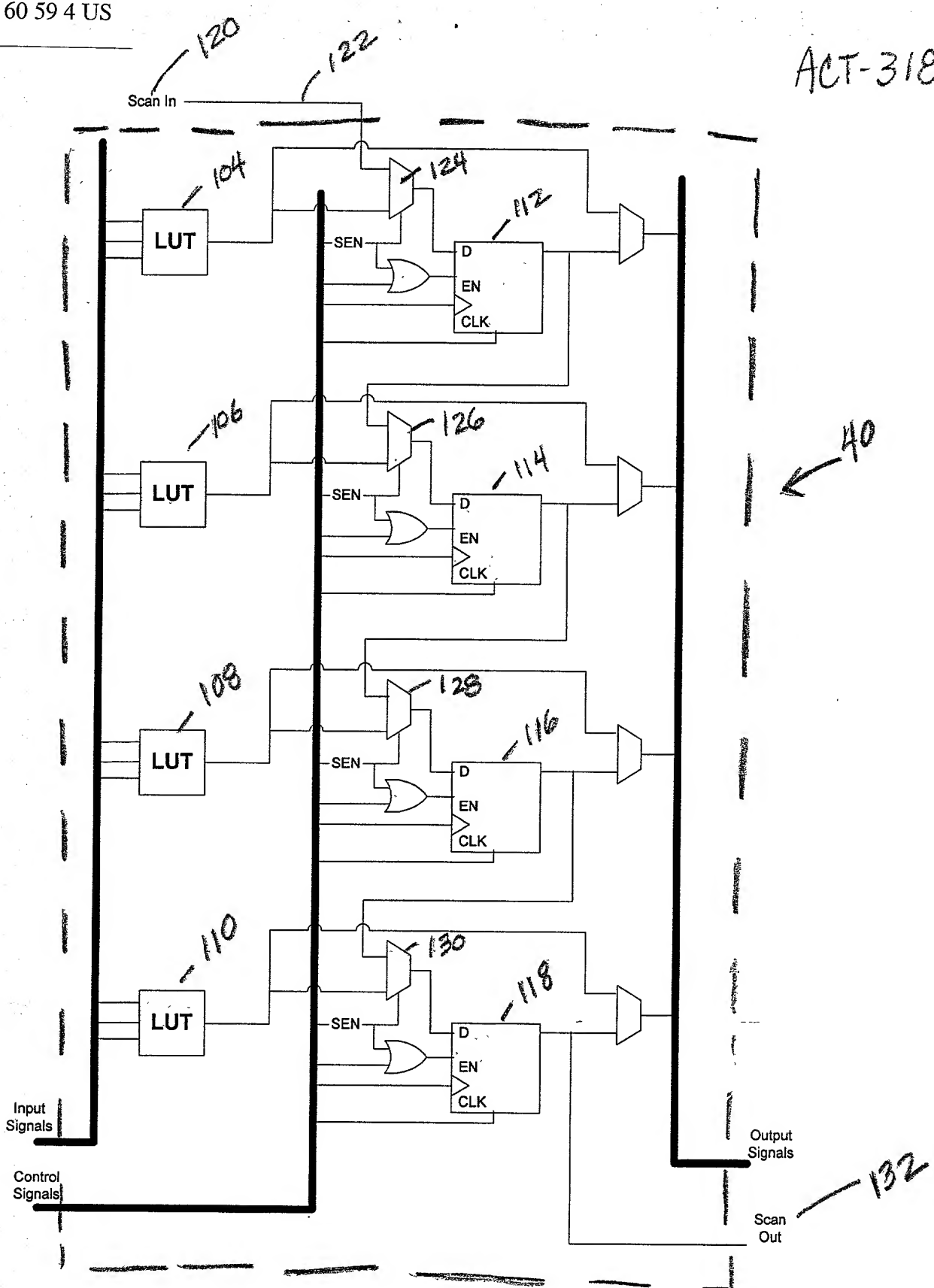


Fig. 9

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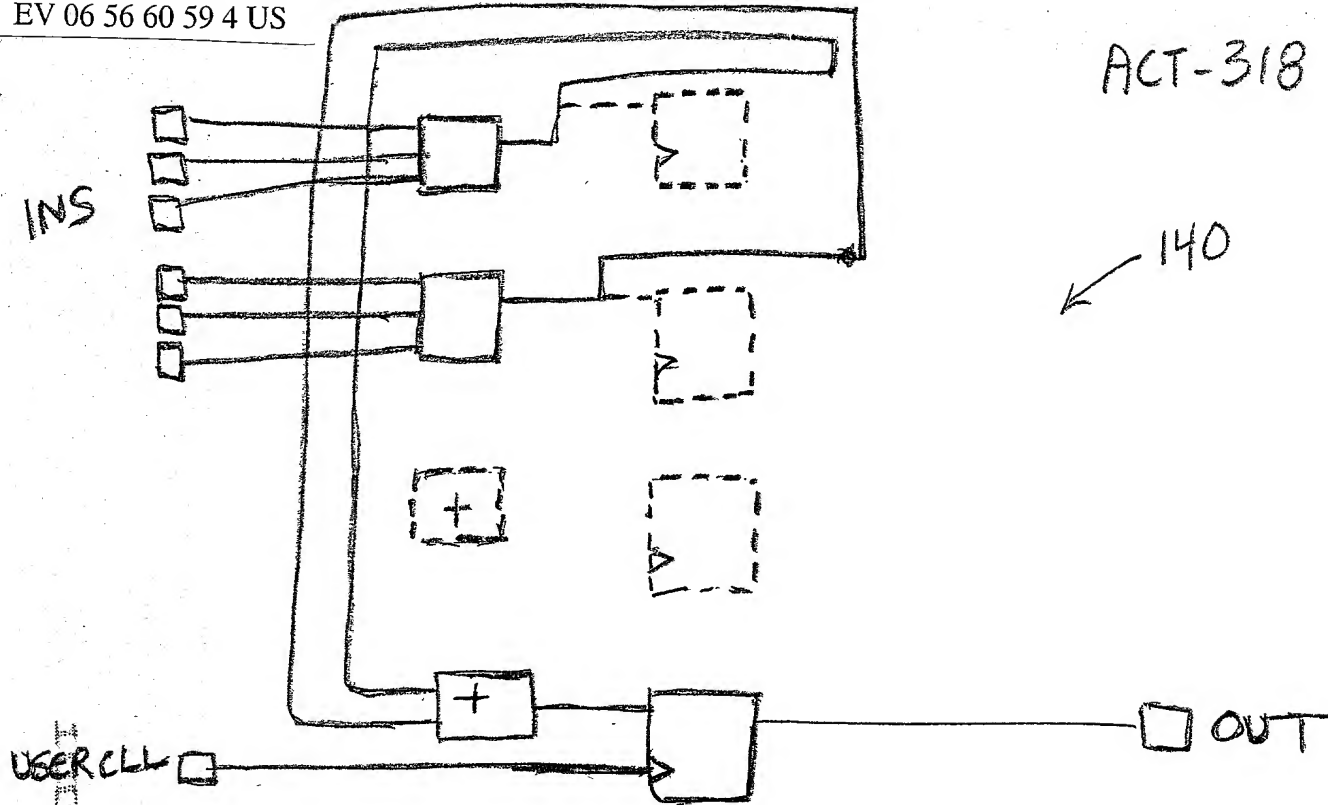


FIG. 10A. USER LOGIC : Implementation of AND OR circuit and register

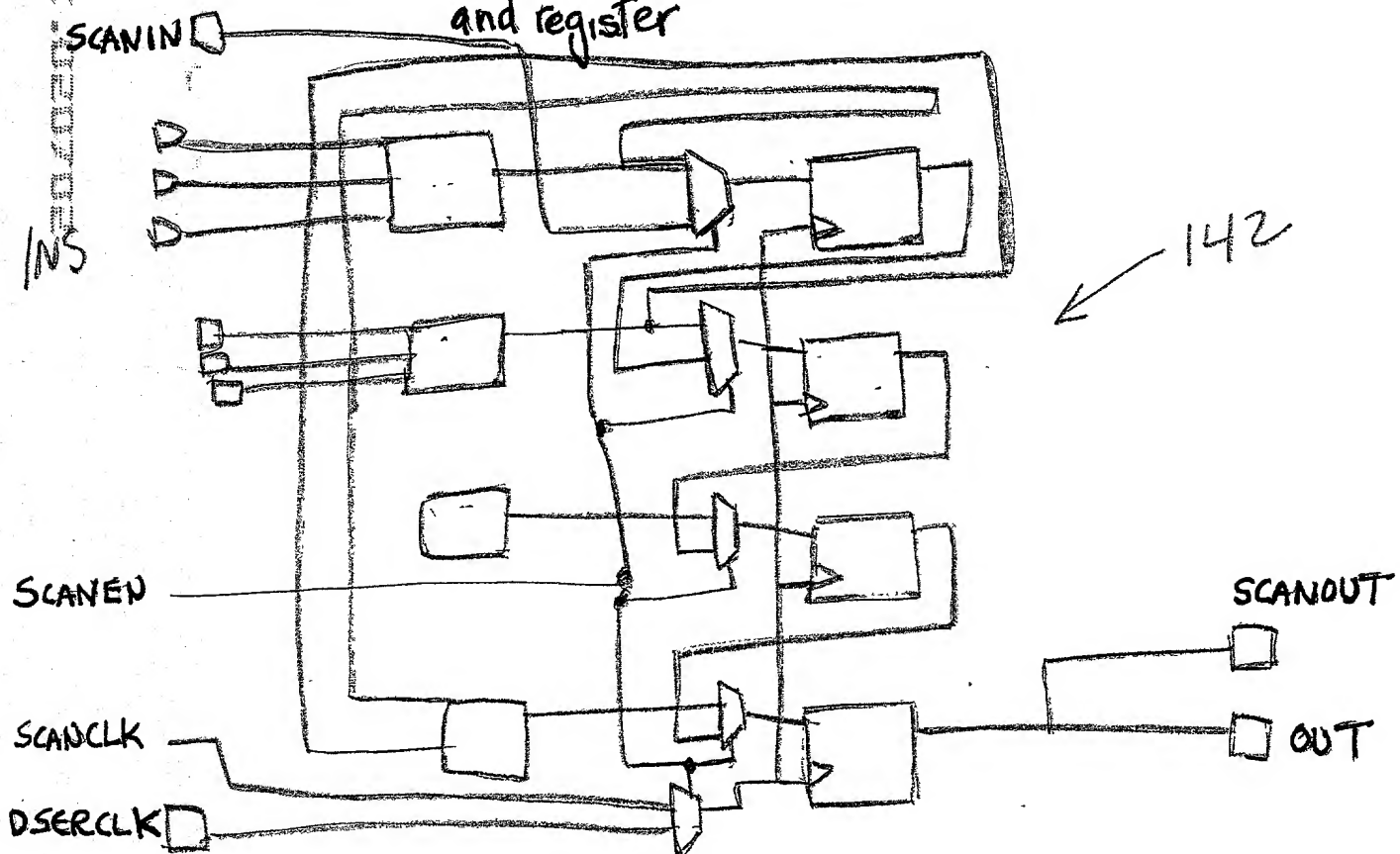


FIG. 10B DSER Logic - With SCAN Superimposed

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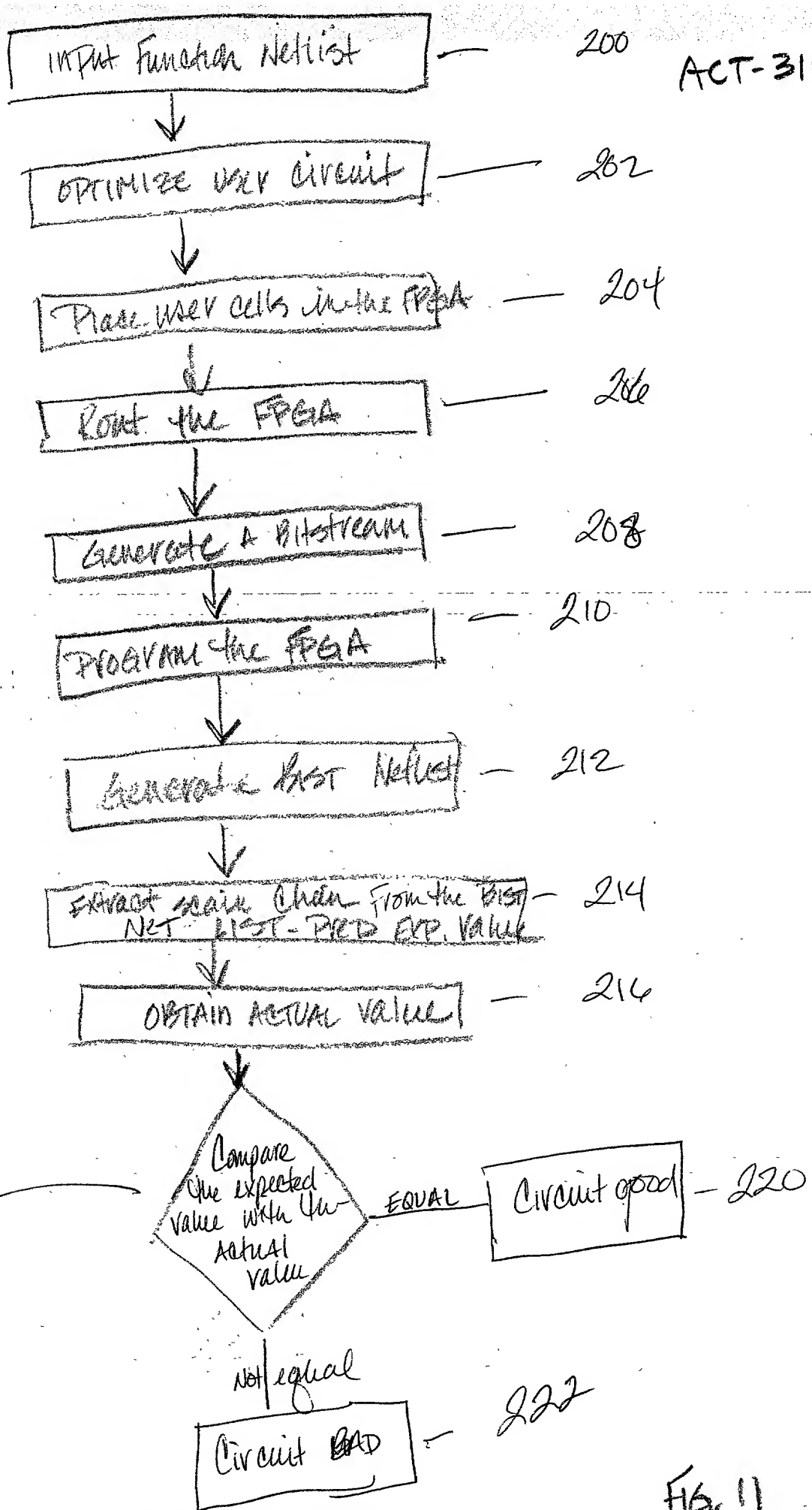


FIG. 11